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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,611	06/03/2005	Masaru Kuramoto	Q88048	4984

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EXAMINER	
KIM, JAY C	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/537,611	KURAMOTO ET AL.	
	Examiner	Art Unit	
	Jay C. Kim	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed October 3, 2007.

Election/Restrictions

1. Applicants' election without traverse of Group I, claims 1-11, in the reply filed on October 3, 2007 is acknowledged. Claims 12-21 are cancelled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tadatomo et al. (US 6,225,650) in view of Motoki et al. (US 2003/0145783).

Regarding claim 1, Tadatomo et al. disclose a nitride semiconductor substrate (Fig. 4) comprising a base substrate (1) (col. 5, line 25 and col. 4, lines 12-15), a mask (2) (col. 5, line 22) formed over the base substrate (1), a semiconductor multilayer film (combined layer of 3 and 31) (col. 5, lines 25-26 and line 30) formed above the mask (2), and the mask (2) is made of non-crystalline material including nitrides (col. 4, lines 27-34) and also formed into a multilayer structure (col. 4, lines 34-35).

Tadatomo et al. further disclose that a GaN crystal (1 in Figs. 9(a) and 10(a)) (col. 8, lines 57-58) can be a group III nitride semiconductor substrate for GaN crystal growth (col. 10, lines 3-9).

Tadatomo et al. differ from the claimed invention by not showing that the group III nitride semiconductor substrate has a dislocation density in the vicinity of the surface thereof of $1 \times 10^7/cm^2$ or less, and that the mask has a polycrystalline material deposited on the surface thereof.

Motoki et al. disclose a group III nitride semiconductor substrate (Fig. 10(5)) formed by GaN single crystal growth (Fig. 10(4)) and then polishing (line 1 of [0312]), which has a dislocation density in the vicinity of the surface thereof less than $1 \times 10^7/cm^2$ (lines 7-8 of [0316]). Motoki et al. further disclose a nitride semiconductor substrate (Fig. 5) where the mask (23) (SiO_2 on line 1 of [0183]) can have a polycrystalline material (polycrystalline GaN on line 2 of [0183]) deposited on the surface thereof.

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor substrate disclosed by Tadatomo et al. with the low dislocation density group III nitride semiconductor substrate and the mask having a polycrystalline material deposited on the surface thereof disclosed by Motoki et al., because the combined nitride semiconductor substrate could be used for improving device characteristics due to low dislocation density of the substrate, and a multilayer mask structure for GaN crystal growth is well-

known and the polycrystalline material would cause different GaN growth kinetics than a single mask structure and thus allow for better control of GaN growth.

Regarding claim 2, Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that the polycrystalline material is formed from a material containing aluminum and nitrogen as essential elements.

Motoki et al. further disclose that the mask (23) can be made of polycrystalline aluminum nitride (AlN) or polycrystalline gallium nitride (GaN) ([0182]).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor substrate disclosed by Tadatomo et al. in view of Motoki et al. with the polycrystalline AlN disclosed by Motoki et al. to make a nitride semiconductor substrate comprising polycrystalline AlN deposited on the mask, because both polycrystalline AlN and polycrystalline GaN can be used to grow high quality single crystal GaN.

Regarding claim 3, Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that voids are formed on the surface of the mask having the polycrystalline material.

Motoki et al. further disclose voids (voluminous defects in voluminous defect accumulating region H in Fig. 5(a)(3)) are formed on the surface of the mask (23) having the polycrystalline material (lines 7-9 of [0299], lines 1-3 of [0420] and lines 11-13 of [0427]).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor substrate disclosed by Tadatomo et al. in view of Motoki et al. with voids formed on the surface of the mask having the polycrystalline material disclosed by Motoki et al., because voids would be formed on a mask while growing single crystal GaN due to imperfect growth of single crystal GaN on an amorphous or polycrystalline material.

Regarding claim 4, Tadatomo et al. further disclose for the nitride semiconductor substrate according to Claim 1 that the mask (2) is provided on the surface of the group III nitride semiconductor substrate (1) (Fig. 4).

Regarding claim 6, Tadatomo et al. disclose a nitride semiconductor device (Figs. 9(a), 9(b) and 10(a)) comprising a group III nitride semiconductor substrate (1) (col. 8, lines 57-58), a mask (2) (col. 4, line 8) formed over the group III nitride semiconductor substrate (1), and a semiconductor multilayer film (combined layer of 3 and k or k1) (col. 4, line 9, col. 10, lines 6-9 and col. 8, line 60) formed above the mask (2), the semiconductor multilayer film (combined layer of 3 and k or k1) including an active layer (k or k1) (col. 10, lines 6-9 and col. 8, line 60), wherein the mask (2) is made of non-crystalline material including nitrides (col. 4, lines 27-34) and also can be formed into a multilayer structure (col. 4, lines 34-35).

Tadatomo et al. differ from the claimed invention by not showing that the group III nitride semiconductor substrate has a dislocation density in the vicinity of the surface

thereof of $1 \times 10^7/cm^2$ or less, and the mask has a polycrystalline material deposited on the surface thereof.

Motoki et al. disclose a group III nitride semiconductor substrate (Fig. 10(5)) formed by GaN single crystal growth (Fig. 10(4)) and then polishing (line 1 of [0312]) which has a dislocation density in the vicinity of the surface thereof less than $1 \times 10^7/cm^2$ (lines 7-8 of [0316]). Motoki et al. further disclose a nitride semiconductor substrate (Fig. 5) where the mask (23) (SiO_2 on line 1 of [0183]) has a polycrystalline material (polycrystalline GaN on line 2 of [0183]) deposited on the surface thereof.

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor device disclosed by Tadatomo et al. with the low dislocation density group III nitride semiconductor substrate and the mask having a polycrystalline material deposited on the surface thereof disclosed by Motoki et al., because the combined nitride semiconductor device would have improved device characteristics due to low dislocation density of the substrate, and a multilayer mask structure for GaN crystal growth is well-known and the polycrystalline material would cause different GaN growth kinetics than a single mask structure and thus allow for better control of GaN growth.

Regarding claim 7, Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that the polycrystalline material is formed from a material containing aluminum and nitrogen as essential elements.

Motoki et al. further disclose that the mask (23) can be made of polycrystalline aluminum nitride (AlN) or polycrystalline gallium nitride (GaN) ([0182]).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor device disclosed by Tadatomo et al. in view of Motoki et al. with the polycrystalline AlN disclosed by Motoki et al. to make a nitride semiconductor device comprising polycrystalline AlN deposited on the mask, because both polycrystalline AlN and polycrystalline GaN can be used to grow high quality single crystal GaN.

Regarding claim 8, Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that voids are formed on the surface of the mask having the polycrystalline material.

Motoki et al. further disclose voids (voluminous defects in voluminous defect accumulating region H in Fig. 5(a)(3)) are formed on the surface of the mask (23) having the polycrystalline material (lines 7-9 of [0299], lines 1-3 of [0420] and lines 11-13 of [0427]).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor device disclosed by Tadatomo et al. in view of Motoki et al. with voids formed on the surface of the mask having the polycrystalline material disclosed by Motoki et al., because voids would be

formed on a mask while growing single crystal GaN due to imperfect growth of single crystal GaN on an amorphous or polycrystalline material.

Regarding claim 9, Tadatomo et al. further disclose for the nitride semiconductor device according to Claim 6 that the mask (2) is provided on the surface of the group III nitride semiconductor substrate (1) (Fig. 9(a)).

Regarding claim 11, Tadatomo et al. in view of Motoki et al. differ from the claimed invention by not showing that the mask is provided in the vicinity of a device separating groove of the nitride semiconductor device.

Tadatomo et al. further disclose that a mask (2 in Fig. 11) is provided in the vicinity of a device separating groove (groove separating the devices in Fig. 11) (col. 10, lines 24-26) of the nitride semiconductor device (Fig. 11).

Since both Tadatomo et al. and Motoki et al. teach a nitride semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the nitride semiconductor device disclosed by Tadatomo et al. in view of Motoki et al. with the nitride semiconductor device disclosed by Tadatomo et al. comprising a device separating groove, because forming a stripe laser comprising a device separating groove is well-known in manufacturing a nitride semiconductor device as well as forming an individual nitride semiconductor device shown in Fig. 9(b) of Tadatomo et al.

Response to Arguments

4. Applicants' arguments filed October 3, 2007 have been fully considered but they are not persuasive.

Applicants argue that "Tadatomo fails to disclose a substrate having a low dislocation density or a mask having a polycrystalline material deposited on the surface thereof", that "Motoki fails to disclose using a substrate having a dislocation density of 1 × $10^7/cm^2$ or less for forming a mask having a polycrystalline material on the substrate", that "neither Tadatomo nor Motoki teaches or suggests that a group III nitride semiconductor substrate having a low dislocation density is used, and a mask having a polycrystalline material is formed over the substrate", that "it is not recognized in Tadatomo and Motoki that the problem of developing many dislocations from the vicinity of the mask is caused", and that "neither Tadatomo nor Motoki teaches or suggests a means for solving the above problem which is particularly caused in case that the group III nitride semiconductor is grown on a substrate having a low dislocation density".

Motoki et al. disclose a nitride semiconductor substrate having a low dislocation density and a mask having a polycrystalline material deposited on the surface thereof as discussed above. The nitride semiconductor substrate comprising a low dislocation density disclosed by Motoki et al. can be combined with the mask having a polycrystalline material on the substrate disclosed by Motoki et al., because it would have been obvious to the one of ordinary skill in the art at the time the invention was made that a nitride semiconductor substrate comprising a low dislocation density could

be used for improving device characteristics, and a multilayer mask structure including a polycrystalline material for GaN crystal growth is well-known.

There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. Therefore, lack of teaching of "the problem of developing many dislocations from the vicinity of the mask is caused" by Tadatomo et al. and Motoki et al. does not necessarily prevent one of ordinary skill in the art at the time the invention was made from combining the references of Tadatomo et al. and Motoki et al.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jay C. Kim whose telephone number is (571) 270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

J.K.
November 15, 2007

Matthew C. Landau
Primary Examiner